In the claims:

Please cancel claims 1-19, without prejudice.

Please amend claims 20-22 and add claims 23-32 to read as follows:

1-19. (Cancelled)

20. (Currently Amended) A video graphics circuit comprising:

a frame buffer, wherein the frame buffers stores display information;

a gamma correction block operably coupled to the frame buffer wherein the gamma correction block stores a plurality of sets of precomputed gamma corrected data corresponding to a plurality of gamma correction curves, wherein the gamma correction block receives the display information from the frame buffer and gamma selection information, wherein the gamma correction block provides gamma corrected data in response to the display information from a gamma correction curve selected by the gamma selection information, outputting a digital display signal including the gamma corrected data; and

a digital to analog converter operably coupled to the gamma correction block, wherein the digital to analog converter receives the gamma corrected data and generates an analog display signal, outputting the analog display signal.

21. (Currently Amended) A video graphics circuit comprising:

a frame buffer, wherein the frame buffers stores display information;

a gamma correction block operably coupled to the frame buffer wherein the gamma correction block stores a plurality of sets of precomputed gamma corrected data corresponding to a plurality of gamma correction curves, wherein the gamma correction block receives the display information from the frame buffer and gamma selection information, wherein the gamma correction block provides gamma corrected data in response to the display information from a gamma

correction curve selected by the gamma selection information, outputting a digital display signal including the gamma corrected data; ~~and~~

a video graphics processor operably coupled to the frame buffer, wherein the video graphics processor generates at least a portion of the display information stored in the frame buffer; and

a digital to analog converter operably coupled to the gamma correction block, wherein the digital to analog converter receives the gamma corrected data and generates an analog display signal, outputting the analog display signal.

22. (Currently Amended) A method for gamma correction in a video graphics system, comprising:

receiving pixel information, wherein the pixel information is generated from display information stored within a frame buffer;

selecting a set of gamma corrected data from a plurality of sets of precomputed gamma corrected data based on the pixel information and gamma selection information, wherein the plurality of sets of precomputed gamma corrected data include gamma corrected data corresponding to a plurality of gamma correction curves; ~~and~~

converting the set of gamma corrected data from a digital format to a portion of an analog display signal; and

outputting a digital display signal including the set of gamma corrected data and the analog display signal.

23. (New) The video graphics circuit of claim 20 wherein the gamma correction block further includes:

a plurality of gamma correction lookup tables corresponding to a plurality of gamma values, wherein each of the plurality of lookup tables provides a set of output data in response to received input data; and

a gamma table selector that receives the set of output data and automatically selects the set of output data corresponding to one of the plurality of lookup tables, wherein the automatic selection of the set of output data is based on the gamma selection information.

24. (New) The video graphics circuit of claim 23 wherein the precomputed gamma corrected data includes a pass through function, wherein the pass through function provides the display information as the set of gamma corrected data.

25. (New) The video graphics circuit of claim 23, wherein the gamma correction curve maps values of the display information to output values on the gamma correction curve.

26. (New) The video graphics circuit of claim 23, wherein a set of pixel data is provided as the display information to each of a plurality of gamma correction tables, and wherein a gamma table selector includes a multiplexor that receives the sets of output data from the plurality of gamma correction lookup tables, wherein the multiplexor selects a selected set of output data from the sets of output data based on the gamma selection information.

27. (New) The video graphics circuit of claim 25, wherein the gamma correction tables are memory structures addressed by the received input data.

28. (New) The video graphics circuit of claim 21 wherein the gamma correction block further includes:

a plurality of gamma correction lookup tables corresponding to a plurality of gamma values, wherein each of the plurality of lookup tables provides a set of output data in response to received input data; and

a gamma table selector that receives the set of output data and automatically selects the set of output data corresponding to one of the plurality of lookup tables, wherein the automatic selection of the set of output data is based on the gamma selection information.

29. (New) The video graphics circuit of claim 28 wherein the precomputed gamma corrected data includes a pass through function, wherein the pass through function provides the display information as the set of gamma corrected data.

30. (New) The video graphics circuit of claim 28, wherein the gamma correction curve maps values of the display information to output values on the gamma correction curve.

31. (New) The video graphics circuit of claim 28, wherein a set of pixel data is provided as the display information to each of a plurality of gamma correction tables, and wherein a gamma table selector includes a multiplexor that receives the sets of output data from the plurality of gamma correction lookup tables, wherein the multiplexor selects a selected set of output data from the sets of output data based on the gamma selection information.

32. (New) The video graphics circuit of claim 31, wherein the gamma correction tables are memory structures addressed by the received input data.